



C E R T I F I C A T E

Certificate registration number: G3.2005.387.2.A4

Certificate holder: Mikroelektronika A.D.

Product designation: MEM600,
Hardware version 982312, Firmware version 5.0

Certification date: May 6th, 2020

This certificate indicates the above mentioned product successfully completed certification testing with regards to the reference specification ITU G.9903 (08-2017). The optional feature coherent mode of the G3-PLC protocol is also covered by this certification.

The certificate applies to certification profile CENELEC A and the device was configured as a PAN-Device.

Test cases have been performed as described in the test report referred to below. This certificate is granted on account of tests conducted by Laboratoire des Applications Numériques (LAN) in Tauxigny, France in April 2020. The results and remarks can be found in the complete test report.

Applied tests	Performed by	Document evidence
Conformance, interoperability and performance testing according to the test specification referenced by the test report	Laboratoire des Applications Numériques (LAN)	LAN19AF0106

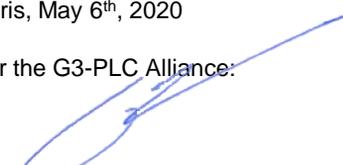
The device tested is a G3-PLC CENELEC A 1-phase meter. The meter is equipped with the G3-PLC certified platform SMG-EV51-A1-EV8000 with certificate no. G3.2002.374.1.A4. The Protocol Implementation Conformance Statement in the Annex includes the PICS related to performance and is an integral part of this certificate. This certificate is valid from May 6th, 2020.

The certificate is only applicable to the product described above and permits the use of the G3-PLC™ logo as laid down in the G3-PLC logo license agreement.

This certificate does not imply assessment of the production. This certificate shall not be defined, or used as a guarantee covering quality of a product which includes G3-PLC. The liability of the Alliance and the test laboratory or any of her representatives is excluded for any damages or losses of the certified company.

Paris, May 6th, 2020

For the G3-PLC Alliance:


Marc Delandre
Chairman


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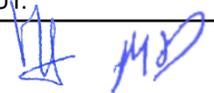
Madeleine Francillard
Chair Certification Program

G3-PLC
Alliance

Annex 1: Protocol Implementation Conformance Statement (PICS)

Feature implementation statement

Name	Value	Description
BAND_PLAN	CENELEC A	Indicate the band-plan supported by the device.
FEATURE_PAN_COORDINATOR	FALSE	Indicate if the device is a PAN-Coordinator (true) or a normal device (false).
FEATURE_COHERENT_MODULATION	TRUE	Indicate if coherent modulation is supported.
FEATURE_EAP_SERVER	FALSE	Indicate if an EAP-PASK server is implemented by the DUT. Apply only if FEATURE_PAN_COORDINATOR = true.
FEATURE_D8PSK_MODULATION	TRUE	True / False
FEATURE_ROUTING	TRUE	Indicate if the routing is implemented by the IUT.
FEATURE_SECURITY	F1	Indicate the security implemented by the device. Possible values are: F1, F2.
FEATURE_ACTIVE_SCAN	TRUE	Indicate if the active scan process is done by the IUT after power-up.
FEATURE_PREAMBLE_COEXISTENCE_MECHANISM	FALSE	Indicate if the preamble-based coexistence mechanism is used by the IUT.



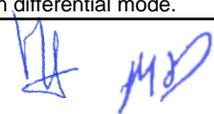
Annex 2: Protocol Implementation Conformance Statement (PICS)

PICS related to performance (1/2)

The device tested is a G3-PLC CENELEC A 1-phase meter.
Testing was performed on phase 1.

Operating voltage applied for certification testing was 230V/50Hz.

Name	Value	Unit	Description
PHY_001_SIGNAL_LEVEL	87	dBµV	Indicate the signal level that can be injected in the band, on a 2 Ohms LISN
PHY_002_SIGNAL_LEVEL	100	dBµV	Indicate the signal level that can be injected in the band, on a CISPR16-1 LISN
PHY_003_SNR_ROBO_D	0.9	dB	SNR level of white noise that can be supported with a FER < 5% for ROBO modulation in differential mode.
PHY_003_SNR_DBPSK	2.5	dB	SNR level of white noise that can be supported with a FER < 5% for DBPSK modulation in differential mode.
PHY_003_SNR_DQPSK	5.7	dB	SNR level of white noise that can be supported with a FER < 5% for DQPSK modulation in differential mode.
PHY_003_SNR_D8PSK	10.1	dB	SNR level of white noise that can be supported with a FER < 5% for D8PSK modulation in differential mode.
PHY_003_SNR_ROBO_C	-0.9	dB	SNR level of white noise that can be supported with a FER < 5% for ROBO modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_003_SNR_BPSK	0.7	dB	SNR level of white noise that can be supported with a FER < 5% for BPSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_003_SNR_QPSK	3.9	dB	SNR level of white noise that can be supported with a FER < 5% for QPSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_003_SNR_8PSK	7.8	dB	SNR level of white noise that can be supported with a FER < 5% for 8PSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_005_NOISE_DURATION_ROBO_D	3900	µs	Duration of the impulsive noise that can be supported with a FER < 5% for ROBO modulation in differential mode.



Annex 2: Protocol Implementation Conformance Statement (PICS)

PICS related to performance (2/2)

Name	Value	Unit	Description
PHY_005_NOISE_DURATION_DBPSK	1500	µs	Duration of the impulsive noise that can be supported with a FER < 5% for DBPSK modulation in differential mode.
PHY_005_NOISE_DURATION_DQPSK	1100	µs	Duration of the impulsive noise that can be supported with a FER < 5% for DQPSK modulation in differential mode.
PHY_005_NOISE_DURATION_D8PSK	250	µs	Duration of the impulsive noise that can be supported with a FER < 5% for D8PSK modulation in differential mode.
PHY_005_NOISE_DURATION_ROBO_C	4000	µs	Duration of the impulsive noise that can be supported with a FER < 5% for ROBO modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_005_NOISE_DURATION_BPSK	2700	µs	Duration of the impulsive noise that can be supported with a FER < 5% for BPSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_005_NOISE_DURATION_QPSK	1700	µs	Duration of the impulsive noise that can be supported with a FER < 5% for QPSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_005_NOISE_DURATION_8PSK	1000	µs	Duration of the impulsive noise that can be supported with a FER < 5% for 8PSK modulation in coherent mode. Apply only if FEATURE_COHERENT_MODULATION is true.
PHY_007_SNR	-3.6	dB	Indicate the SNR level that can be supported by the DUT so PHY header (FCH) are correctly decoded (with less than 10% of loss)
PHY_008_SIGNAL_LEVEL	45	dBµV	Indicate the signal level of a frame that can be received correctly by the DUT (with FER<10%)
PHY_009_LQI_MIN_RANGE	40	-	Lower value of LQI to be tested during test PHY_009
PHY_009_LQI_MAX_RANGE	100	-	Higher value of LQI to be tested during test PHY_009
BOOTSTRAP_001_DURATION	67	ms	Duration needed for the DUT to reply to bootstrap messages EAP-PSK #1 and #3. Apply only if FEATURE_DEVICE_TYPE = PAN-Device
BOOTSTRAP_002_DURATION	n/a	ms	Duration needed for the DUT to reply to bootstrap messages joining, EAP-PSK #2 and #4. Apply only if FEATURE_EAP_SERVER is true
BOOTSTRAP_003_DURATION	71	ms	Duration needed for the DUT to relay bootstrap messages. Apply only if FEATURE_DEVICE_TYPE = PAN-Device
TONE_MAP_001_FER	0	%	The Frame Error Rate that can be expected when applying the tone-map configuration provided by the DUT
TONE_MAP_002_DATARATE_1	3400	bits/s	The data-rate that can be expected when applying the tone-map configuration provided by the DUT in situation #1
TONE_MAP_002_DATARATE_2	1700	bits/s	The data-rate that can be expected when applying the tone-map configuration provided by the DUT in situation #2
TONE_MAP_002_DATARATE_3	3200	bits/s	The data-rate that can be expected when applying the tone-map configuration provided by the DUT in situation #3
TONE_MAP_002_DATARATE_4	4000	bits/s	The data-rate that can be expected when applying the tone-map configuration provided by the DUT in situation #4
MESH_ROUTING_001_DURATION	122	ms	Duration needed for the DUT to relay short mesh routed data frames
MESH_ROUTING_002_DURATION	121	ms	Duration needed for the DUT to relay maximum size mesh routed data frames

Annex 3: Copy of test report cover sheet



G3-PLC Certification Test Report			
Mikroelektronika	MEM600 HW:982312 FW: 5.0		
LAN19AF0106	Ed.01	May 4, 2020	Page 1/45

G3-PLC Alliance
G3-PLC Product Certification Test Report

Vendor Name **Mikroelektronika A.D.**
 Model Name **MEM600**
 Serial N° **12000123**
 HW version **982312**
 FW version **5.0**

Test Report # **TR_LAN19AF0106 Ed.01**
 Date **May 4, 2020**

CONF Tests Specification	version 0.30.	03/12/2018
CONF Tests Suite	version 2.9.p1.	09/2019
IOT Tests Specification	version 0.13.	28/12/2018
IOT Tests Suite	version 2.6.p1.	09/2019
PERF Tests Specification	version 0.27.	05/03/2019
PERF Tests Suite	version 2.9.p1.	09/2019

Test Tool **version 2.3**
 Tester Modem **version 2.0**
 Certification Test Procedures **version 1.14** **21/09/2019**

Certification Profile **A (CENELEC A)**
 Role **Meter**
 Overall Verdict **PASS**



Initiation	Date	Description of modification	Ed.
Omar DIOUF	April 30, 2020	Creation	00
Omar DIOUF	May 4, 2020	LQI MIN RANGE PICS updated	01

	Realised by	Checked by	Approved by
Name	Omar DIOUF	Vincent BUCHOUX	Thierry DOLIGEZ
Date	May 4, 2020	May 4, 2020	May 4, 2020
Sign			

The current report and the test results produced in this current are given for information only and must not be relied on by any third person for any reason.
 This report contains an assessment of the apparatus carried out on samples submitted to the laboratory. The results in this report relate only to the items tested and were obtained in the period between the initial receipt of samples and the issue of the report. It should be noted that technical hardware or software modifications on the apparatus may impact the results reported in this document.



Annex 4: Additional details of the platform on which the product is based

Platform model name on which product is based:	SMG-EV51-A1-EV8000
Platform G3-PLC certificate number:	G3.2002.374.1.A4
Exact part number of all the chips running G3-PLC stack in the certified platform:	EV8000ILPT
What each part number runs: lower MAC (incl. CSMA/CA) or PHY or other parts of the stack:	PHY, MAC and 6LowPAN
Hardware version of this chip:	EV8000
Software version running on this chip:	5.0
Internal CPU frequency:	240 MHz